DEADTIME REDUCTION IN THERMAL NEUTRON COINCIDENCE COUNTER

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Two areas for reducing coincidence deadtime have been investigated, analog and digital. The analog work includes use of a commercially available hybrid preamplifier discriminator useful to at least 150 kpps/channel with present detectors and added circuitry for combining multiple channels. The digital work includes reducing OR gate deadtime and the introduction of a derandomizing buffer at the input of the shift-register section, providing benefits to 1 Mpps. The combined efforts of this work have reduced the six-channel coincidence deadtime from ~ 2.4 to ~ 0.7 μs.

1. Introduction

A new, faster amplifier and a derandomizing buffer have been investigated as a means of reducing deadtime in thermal neutron coincidence counters. The amplifier–discriminator is incorporated in the detector junction box. The output logic pulses may be combined with additional amplifier outputs in an integral daisy-chain OR gate. Connection is then made to the shift-register counting system. Also, there is provision for independently disabling each channel. Each amplifier channel is provided with an output monitor lamp.

The derandomizing buffer stores closely spaced logic pulses from the amplifiers until an empty stage is available in the shift register, which occurs every 0.5 μs. This reduces counting losses in the digital section. The buffer also replaces the present synchronizer function. It is implemented on a small printed circuit (PC) board that can be plugged into the existing shift-register board. It is useful to 1 Mpps with the present shift-register circuitry. [1]

Either of these two changes will result in a 30% to 40% reduction in coincidence deadtime. Used together, they will reduce coincidence deadtime by a factor of 3 to 4. Sect. 2 of this report will discuss the amplifier design and measurements. Sect. 3 discusses the derandomizing buffer and its implementation.

2. New amplifier design

Several new features (improvements of the original design) [1] have been incorporated in this design.

2.1. Brief description of new features

1. Same box: The preamplifier–amplifier–dis-criminator system is mounted in the same box as the detectors. High- and low-voltage components and connectors are separated by a shield plane.

2. Complete counter: Each detector–amplifier bank is complete: that is, the detector, amplifier discriminator, and digital output are self-contained and capable of supplying transistor–transistor logic pulses to any desired counting system.

3. Or output: Provisions are made for combining outputs of multiple channels.

4. Output monitor: Each detector–amplifier bank has an output monitor lamp.

5. Single 5 V supply: The unit requires a single +5 V supply and a highvoltage supply for the ^{3}He detector.

6. Enable feature: Provision is made for disabling individual channels.

2.2. Amplifier circuit board configuration

1. General description: The amplifier board, which contains three integrated circuits (fig. 1), is composed of an analog section and a digital section. The integrated circuits are: an AMPTEK A-111 * hybrid charge pre-amplifier–discriminator, a 74221 dual one-shot, and a 74-S 140 dual four-input 50-Ω line driver. These are contained on a 1.5- by 2.2-in. PC board.

2. Analog section: Back-to-back diodes are provided at the input of the A-111 for input protection. A gain control is provided to match gains in multichannel systems. An amplifier test point included on the board has been used for diagnosing noise problems.

3. Digital section: The A-111 discriminator digital output is too wide (~ 0.3 to 0.5 μs) to OR directly with other channels. One section of the 74221 shortens this

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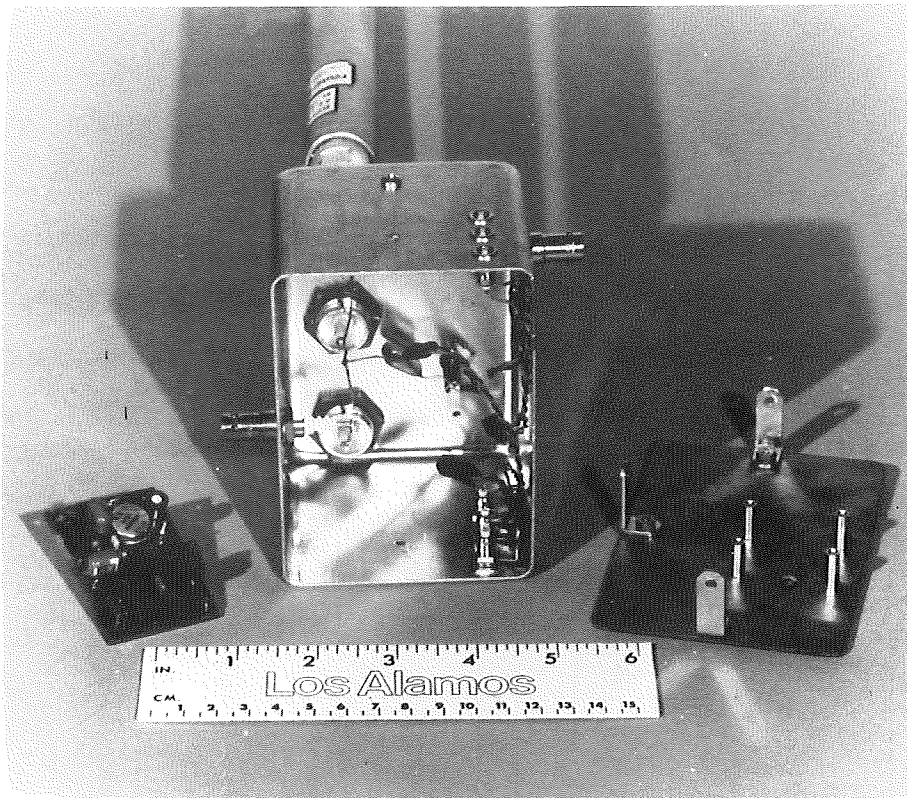
* AMPTEK, Inc., Bedford, Massachusetts, USA.

Fig. 1. Amplifier board with shield plane in single-channel application.

output to 50 ns. A potentiometer is provided to adjust output pulse widths. The other section provides a 3-ms pulse to drive the output monitor lamp. Output may be disabled by opening the connection between two pins on the B connector.

4. OR gate: The 74-S 140 functions as a two-input logic OR gate, combining logic pulses from this board with output pulses from a second board and passing the combined output to a third board in daisy-chain fashion as illustrated in fig. 2. The unused input at the beginning of the daisy chain must be held at a logic low to enable the daisy chain. The OR ouput (pins B 7, 8) of
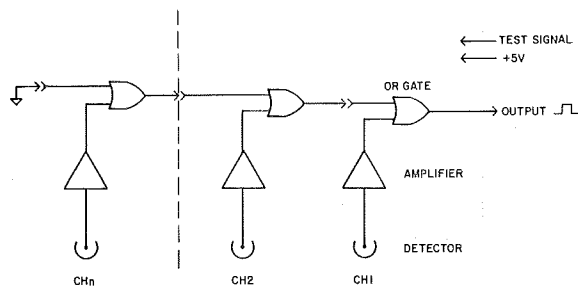

Fig. 2. "Pipelined" or daisy-chain OR gate.

each board is series terminated in 50 Ω. The OR input pins are B 1, 2.

5. Power and ground: Analog and digital grounds are handled differently, and care must be used to ensure that digital ground currents do not mix in sensitive areas, that is, in paths that are common with the detector input signal. As mentioned above, the board is divided into two sections. analog and digital, and separate unconnected ground planes are provided. When the grounds are properly implemented, only analog currents flow in the analog ground, and digital ground currents are supplied by another path. This prevents feedback through common impedances that causes multiple pulsing or oscillation.

6. Output monitor lamp: The output monitor is designed to flash for any pulse that exceeds the threshold of the A-111. It is driven by the logic AND of the A-111 and the OR output. This ensures that the lamp flashes only if both analog and digital sections are functional. The lamp also is turned off if the disable feature is used. In addition to verifying board operation, the lamp has proved useful for matching gains in multichannel systems and for diagnosing induced-noise problems. The light-emitting diode is connected to pins 5 and 6 on the B connector; pin 6 is the anode.
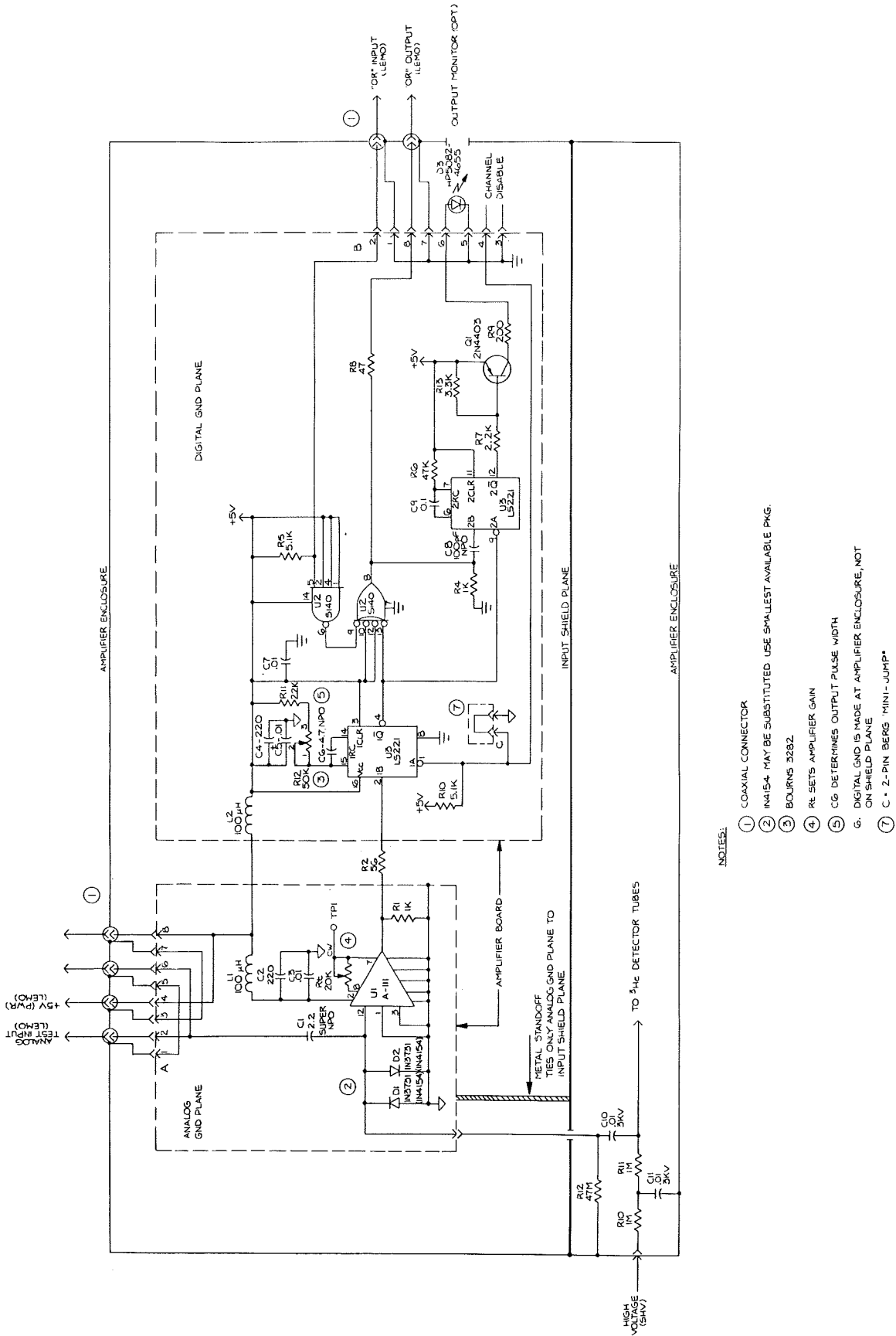
Fig. 3. Schematic and wiring of a single amplifier/enclosure.

2.3. Amplifier circuit board implementation

1. Shield plane: A shield board (fig. 1) is required to prevent output signal feedback through the exposed anode connections of the detectors. This shield board, made from a double-sided PC board, divides the amplifier enclosure logically into two compartments. All high-voltage components and connections are located under the board, and all low-voltage components are located above it. The detector signal is fed through the shield by a pin jack and plug mounted on an insulating stand-off. Fig. 3 shows conceptual wiring and schematic of a single amplifier per enclosure.

2. Ground, power, and enable connections: An eight-pin Berg connector labeled A allows busing of +5 V and a test input signal and their respective shields. The analog 5-V common is supplied through the metal stand-offs supporting the amplifier board. The digital 5-V common is supplied by the eight-pin Berg connector labeled B (odd-numbered pins are digital common), is bused along with the OR input (1,2) and output (7,8), and is connected to the amplifier enclosure at the signal connec-

tor. This prevents ground loops inside the enclosure. The test input is to verify operation of the amplifier, not to calibrate gain. If the test input is bused for use in a detector system, it should be terminated in a low impedance (that is, 50 Ω) to prevent the output signal from coupling into the preamplifier input. A channel may be disabled by opening the connection between pins 3 and 4 on the B connector.

3. Single amplifier / enclosure: The prototype units shown in fig. 4 are connected within the boxes using twisted-pair cable routed close to the inside wall of the boxes to reduce signal radiation. Between the boxes, RG-174 cable with K-lock connectors is used. This configuration seems to work well. Crosstalk between channels has not been a problem where only twisted-pair cables were used.

4. Multiple amplifier / enclosure: In applications where multiple channels are incorporated in one enclosure, it will be necessary to use shielded cable (that is, RG-174) inside the enclosure.

2.4. AMPTEK A-111

1. General description: the Model A-111 is a commercially available hybrid charge-sensitive preamplifier, discriminator, and pulse shaper developed by AMPTEK, Inc., for use with low-capacitance, charge-producing detectors. These devices are designed for use with fast detectors such as photomultiplier tubes and electron channel multipliers; however, they have sufficient gain and low enough noise to be used with the slower ^{3}He detectors at the expense of realizing full count-rate capability. Operating with the high voltage at approximately 1700 V improves the signal-to-noise ratio and allows a sufficient range of gain adjustment for matching of multiple channels.

2. Threshold level and gain: The threshold adjustment referred to in the A-111 data sheet is in fact an amplifier gain adjustment. The range of adjustment ~ 10 : 1 is accomplished by a 20-KΩ potentiometer connected between pins 7 and 8. Normally, gain is set once during fabrication of the detector assembly. First all channels are matched and, then, the gain of all channels is raised or lowered to the desired operating point using the high voltage. Gain is set so that the threshold is in the "valley" between the gamma and neutron regions of the ^{3}He pulse-height spectrum.

2.5. Measurements

1. Pulse shaping in the AMPTEK A-111: Fig. 5 shows the pulse shape from pin 7 of the A-111 with an AmLi source. This and pulser tests show the time constant to be equivalent to an amplifier with single RC integration and differentiation time of ~ 0.15 μs. Further information from AMPTEK, Inc., indicates that the amplifier
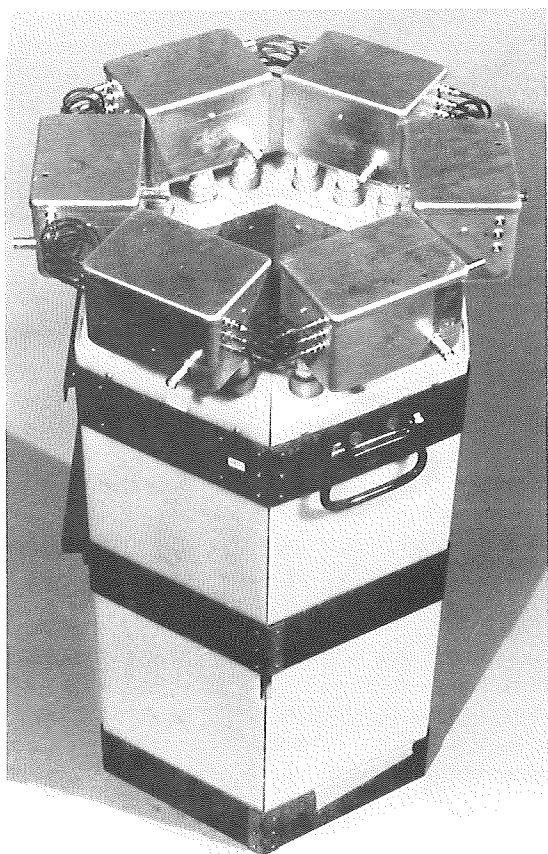

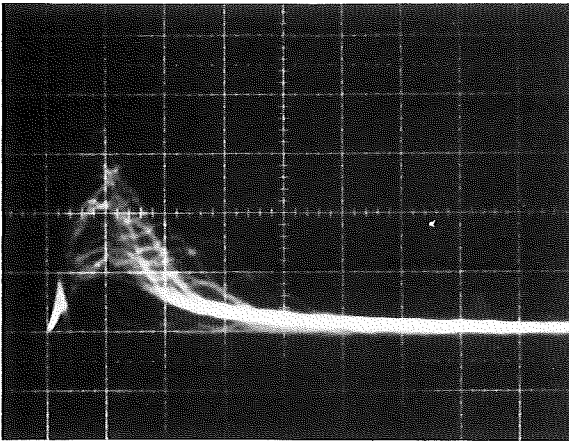Fig. 4. Prototype HLNCC with six separate amplifier enclosures.

Fig. 5. Pulse shape from ^{3}He detector; horizontal scale = 0.5 μs/division and vertical scale = 50 mV/division.

output is connected internally to the discriminator by a 0.3-μs coupling time constant. Although this second differentiator is somewhat longer than customary, usually both differentiators have the same constant. It may be a good compromise considering that less gain is lost and the time constant is still short enough to prevent baseline shift at rates obtainable with these detectors.

Because of the relatively long charge-collection time in the ^{3}He detectors (0.5–2 μs), the A-111 is operating as a current amplifier. The length of the pulse is determined by the charge-collection time of the detector.

2. Pulse-height spectrum with A-111 and 2.54-cm-diam. ^{3}He detectors: Fig. 6 shows two pulse-height spectra at pin 7 of the A-111. Two rates, ~ 5 kpps and 56 kpps, show baseline shift. This was believed to be a basic limitation of the A-111 until further information from AMPTEK, Inc., indicated pin 7 was connected internally to the discriminator through a 0.3-μs differentia-
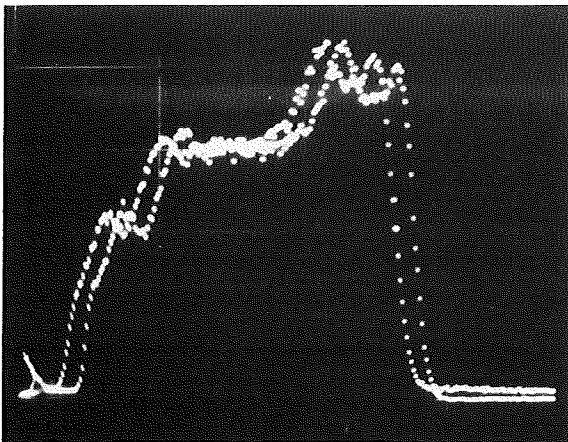

Fig. 6. Two pulse-height spectra, at 5 kpps and 56 kpps/channel, overlapped and showing a baseline shift.

tor. Fig. 7 shows the pulse-height spectra at the same two rates with a 0.3-μs differentiator added between pin 7 and the pulse-height analyzer. Notice that there is no baseline shift. Although the pulse heights are redistributed toward the low-energy end of the spectra, the minimim-energy neutrons fall at approximately the same point in the spectra.

Since the discrimination level is set in the valley between the gamma and neutron portions of the spectra (fig. 7), the shape of the neutron pulse-height spectra is unimportant.

3. Bias measurements: Bias in the shift-register coincidence counter is defined as a difference between the $R + A$ and A counting rates * when a random source such as AmLi is used. More specifically, % bias = 100 R/A.

Sources of bias are numerous; noise, uncompensated pole zero, even deadtime will generate a bias if the predelay * is not properly set. The bias referred to here is due to amplifier baseline displacement following a pulse. Pulses occurring on this displaced baseline have a different probability of being recorded than pulses occurring much later. If the displacement extends into the $R + A$ gate, then a bias either positive or negative will result.

The previous high-level neutron coincidence counter (HLNCC) design using six channels of 0.5-μs bipolar shaping requires 4.5 μs of predelay to reduce bias to less than 0.01%.

Six channels using the A-111 amplifier require ~ 3 μs of predelay to reduce bias to less than 0.01%. These measurements are taken with a 32-μs gate. We believe this bias is caused by residual charge that is being collected over a period longer than 3 μs and keeping the baseline displaced.

4. Deadtime measurements: The deadtime referred to is the coincidence deadtime measured by using a fixed ^{252}Cf source and a variable random rate provided by AmLi. Coincidence deadtime is determined by the function $\delta(T)$, which is measured by adding random sources to a fixed ^{252}Cf source and by requiring that the corrected "reals" rate remain constant.

A series of measurements was made to determine the deadtime coefficient. The value of

$$\delta(T) = 0.608 + 0.236 \times 10^{-6} T (\text{meas.}) \mu s$$

was derived from a fit to the data [2] for a six-channel system.

Fig. 8 shows the decrease in the measured "Reals" rate as a function of "Totals" rate when only the random rate from AmLi is changed. Fig. 9 shows the

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* Full descriptions of the meaning of $R + A$, A, and "predelay" are beyond the scope of this paper. Refer to the descriptions in ref. [1].
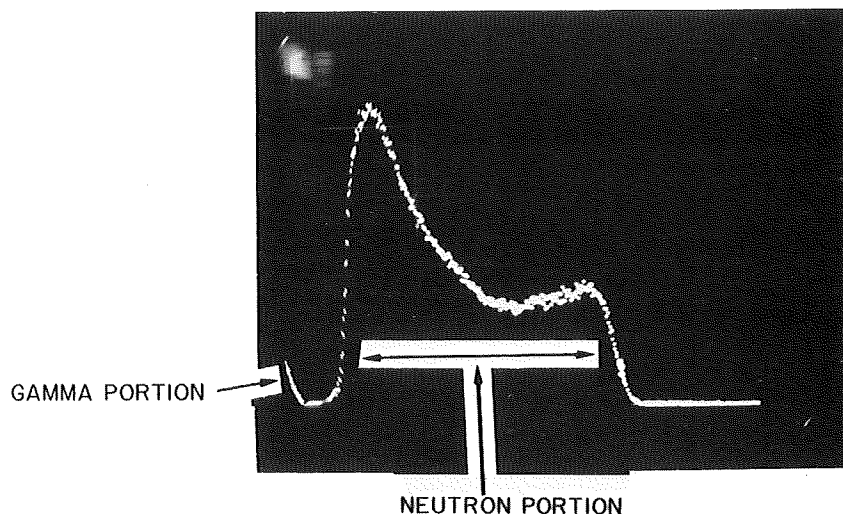
GAMMA PORTION

NEUTRON PORTION

Fig. 7. Pulse-height spectra as seen by the discriminator, showing no baseline shift.

deadtime coefficient $\delta(T)$, which is defined from the relationship

$$R(\text{corrected}) = R(\text{meas.}) \; e^{\delta(T)T(\text{meas.})}.$$

Previous measurements with six channels of the original 0.5-μs bipolar design [1] resulted in a $\delta(T)$ of 2.2–2.4 μs. Six channels of the A-111 design resulted in a $\delta(T)$ of 1.3 μs or a 40% reduction in deadtime. This reduction is disappointing considering that amplifier time constants had been reduced by more than 200%. Obviously a significant portion of the deadtime was being produced by something other than the amplifiers. A method for measuring the coincidence deadtime of the digital section was found. A ^{252}Cf source was placed in the six-channel counter to establish a reference "reals" rate. A digital random pulser [3] was connected to the OR gate and used to increase the random "totals" rate as was done with the AmLi.

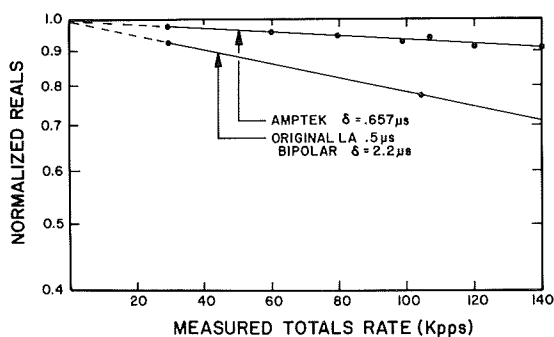Since the "reals" rate coming into the OR gate from the amplifier is not affected by the random pulser, then

Fig. 8. "Reals" response vs "totals" for old and new electronics.

any decrease in the measured "reals" rate is due to deadtime in the digital section, that is, the OR gate and shift-register input synchronizer. When $\delta(T)$ was calculated as above, the deadtime was found to be 1.01–1.11 μs depending on how many banks were OR'd together. Because it takes at least two stages of shift register to make a coincidence and each stage represents 0.5 μs (2 mHz clock), this seems logical.

In the past it was not realized that the digital section contributed such a large fraction to the system deadtime.

3. Derandomizing buffer

3.1. Brief discussion of buffer

The shift-register synchronizer can accept only pulses separated by 0.5 μs or more without counting losses. The original design [1] was capable of supplying pulses separated by 150 ns, but the A-111 is capable of supplying pulses separated by 50 ns. Obviously the 0.5-μs synchronizer is the dominant contributor to digital deadtime.

The function of the derandomizing buffer is to reduce the synchronizer deadtime by accumulating pulses separated by less than 0.5 μs and holding them in store while the slower 0.5-μs shift-register logic catches up. The average interval must be more than 0.5 μs, or count losses will occur. The larger the buffer store, the closer the average interval can approach the resolving time of the shift register without counting losses.

The buffer described here has a store of 16 counts. This allows counting to 1 Mpps with virtually no synchronizer counting losses. Fig. 10 shows a comparison of "totals" losses with and without the buffer, using a random pulser for input.
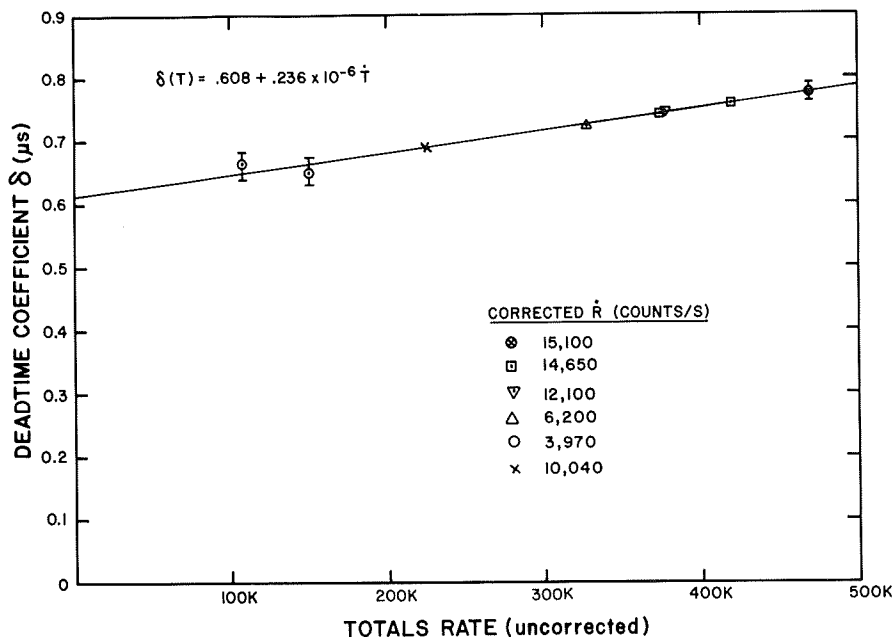
Fig. 9. Dead time coefficient $\delta(T)$.

This reduction in deadtime is not gained without sacrifice, however. Buffer limitations are discussed in sect. 3.3.

3.2. Operation

Fig. 11 shows the buffer operation. If 4-bit counters A and B are both initially reset, counter A counts OR'd amplifier pulses. Resolving time is limited only by the width of the OR pulse. When the first pulse is counted in A, A becomes not equal to B, and the D input of FF_2 is enabled (Lo enables). When CK (2 MH_2 clock signal)

Fig. 10. "Totals" losses with and without the derandomizing buffer, using random pulser at the shift register in connector.

occurs, Q_2 goes high, synchronized with the clock. When CK 1/2 goes high, ~ 350 ns later, Q_2 goes low, incrementing the B counter. A and B are again equal, and D input is disabled.

If several pulses are accumulated rapidly in A, the comparator will simply hold D input enabled until counter B catches up with A. When A overflows, B must also overflow to maintain equality; therefore, no counts are lost.

3.3. Limitations

The derandomizing buffer prevents pulses from being lost by rearranging or stretching them out in time. This tends to produce groups of pulses that get loaded into the shift register as contiguous strings of pulses. As the "totals" rate increases, these strings of pulses become longer and more numerous. When these strings become longer than the predelay in sufficient numbers, then a measurable positive bias will develop. This correlation occurs because the predelay is full and the next input pulse is forced into correlation with a pulse leaving the predelay and entering the "reals" gate. Fig. 12 illustrates the effect of this correlation. Based on these data and the fact that the A-111 amplifier requires 3 μs of predelay, the maximum recommended "totals" rate for less than 0.01% bias is 500 kpps.
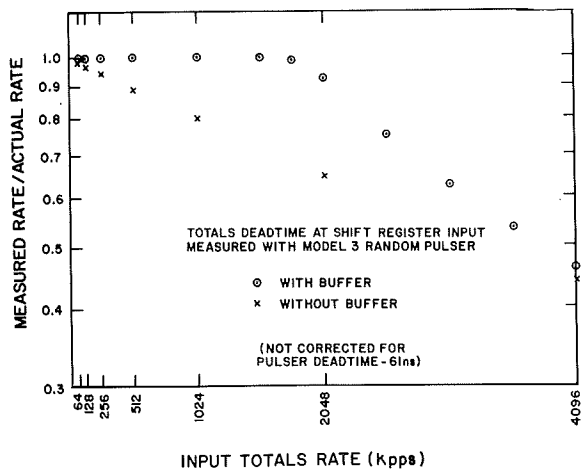
3.4. Implementation

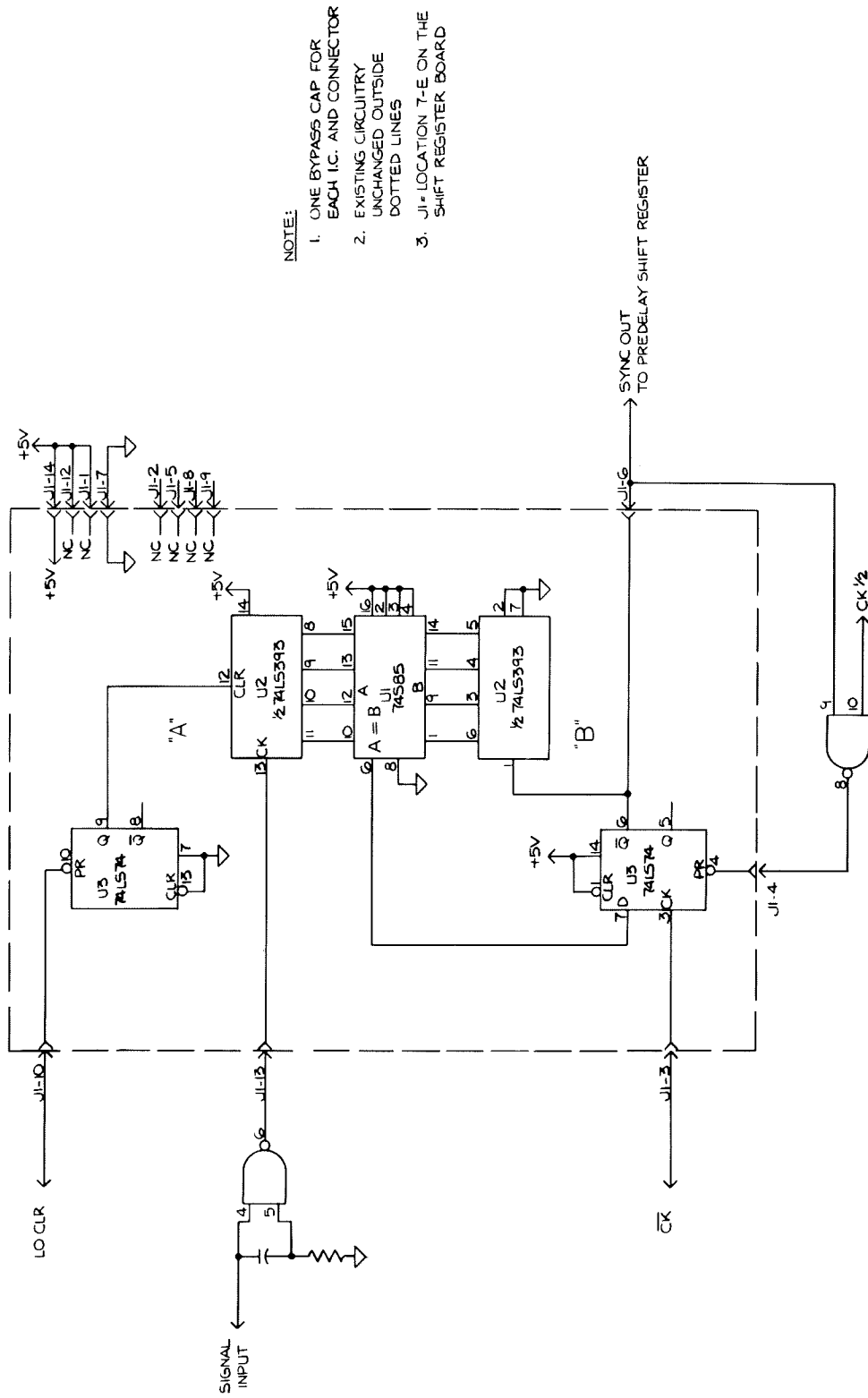The circuit is contained on a 1- by 3-in. PC board shown in fig. 13. The 14-pin header plugs into the
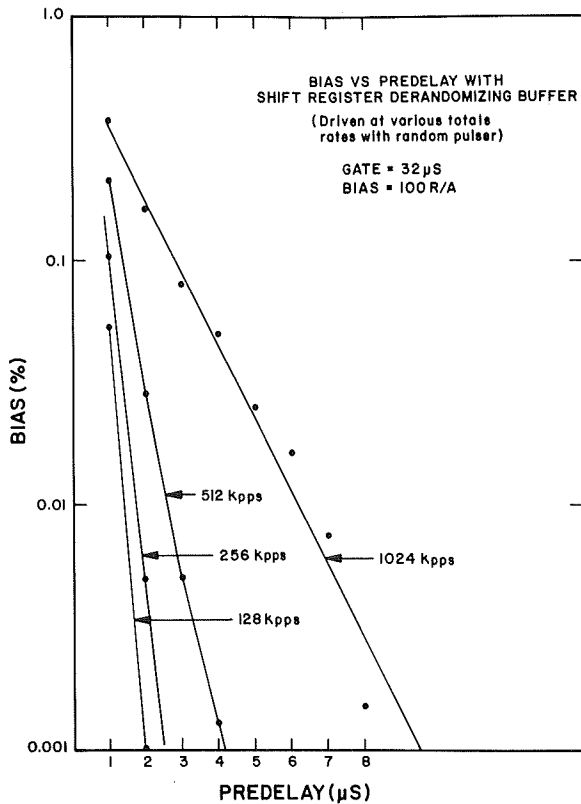
Fig. 11. Derandomizing buffer.

Fig. 12. Bias vs. predelay at various "totals" rates, using random pulser at the shift-register input.

Fig. 13. The derandomizing buffer installed on shift-register board.

synchronizer chip location (7 E) on the shift-register board.

To minimize chip count, the A counter clear signal is provided by the unused 74-LS 74 connected as an inverter.

If used with the original 0.5-μs bipolar amplifier board, the one-shots feeding the OR gate must be reduced to 50 ns to realize the full benefit of the ~ 35% reduction in $\delta(T)$. When used with the A-111 amplifier, the amplifier output is fed directly to the shift-register board.

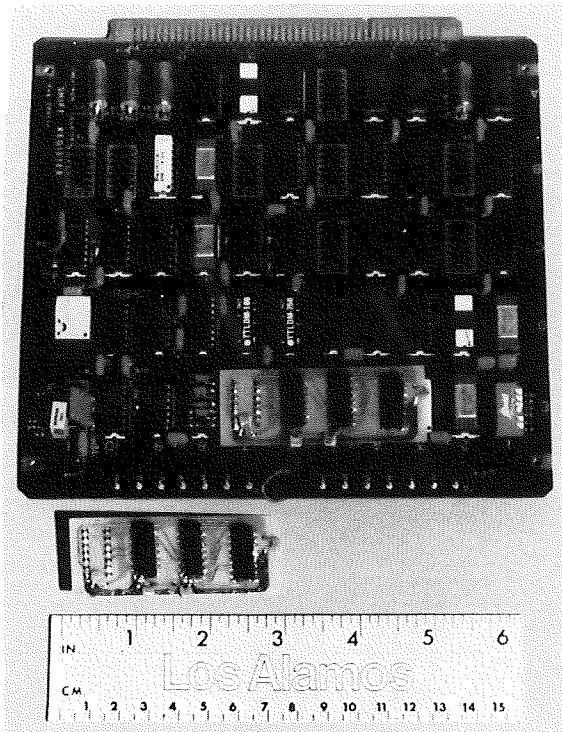I would like to thank the following people for their help: Rebecca Whitehill, for preparing the illustrations for this report; Donna Peterson, for wiring the prototype detector assembly and subsequent assemblies; Ray Holbrooks, for ensuring that the design of the more advanced assemblies incorporated my ideas; and Howard Menlove, for encourgement and for time spent testing the more advanced units.

References

[1] J.E. Swansen, P.R. Collisnworth, and M.S. Krick, Los Alamos Scientific Laboratory report LA-8319-MS (April 1980).
[2] H.O. Menlove, Los Alamos National Laboratory memorandum Q-1-83-461/0070H to M. Baker (July 1983).
[3] J.E. Swansen and N. Ensslin, Nucl. Instr. and Meth. 188 (1981) 83.